UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,319	01/28/2000	Samson Huang	INTL-0312-US (P7995)	2102

7590 12/18/2002

Timothy N Trop
Trop Pruner Hu & MIles PC
8554 Kathy Freeway Ste 100
Houston, TX 77024

EXAMINER
JORGENSEN, LELAND R

ART UNIT	PAPER NUMBER
2675	9

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/493,319	HUANG, SAMSON	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 19 - 44* is/are pending in the application.

4a) Of the above claim(s) *2 - 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 19 - 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on September 25, 2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/493,319 is acceptable and a CPA has been established. An action on the CPA follows.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "60" has been used to designate both "memory" on page 6, line 25, and "bit latches" on page 4, line 26, page 5, lines 3, 6, and page 6, line 4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 20, 27, 34, and 42 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Dependant claims 19, 26, 33, and 40 each

describe that the second digital indication is communicated from the second memory. Dependant claims 20, 27, 34, and 42 broadens rather than narrows the dependant claim by adding that the second digital indication is **not** communicated from the second memory.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 19 – 44 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 19 – 44 describe a first memory and a second memory. The specifications describe only a memory 66.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 19 – 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19

Claim 19 recites the limitation "the second digital indication" and "the second memory" in lines 3 and 4. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, it will be assumed that claim 19 should read as follows:

19. (Proposed) A method comprising:

providing a capacitor to maintain a terminal voltage of a pixel cell near a predetermined voltage;

providing a first memory to store a first digital indication of the predetermined voltage;

providing a second memory separate from the first memory to store a second digital indication of an updated voltage;

during a frame update operation, communicating the second digital indication from the second memory to update the terminal voltage of the pixel cell; and

during a refresh operation, converting the first digital indication into an analog voltage to update a charge on the capacitor.

Claims 20 - 25

Claims 20 – 25 are rejected as dependant on indefinite claim 19.

Claim 25 is also rejected as indefinite for using the term "are associated with." This term fails to define the relation between the different rates and the refresh and frame update operations.

Claims 22 - 24, 30 - 32, and 37 – 39

Claims 22, 23, 36, 37, and 39 recite the limitation "the memory." Claims 30 and 31 recite the limitation "the memory buffers." Claims 23, 24, 31, 32, 37 – 39 recite the limitation "the digital indication(s)" There is insufficient antecedent basis for these limitations in the claim. These claims are dependant on claims that define a first and second digital indication(s), a first and second memory, or first and second memory buffers. It is unclear whether the term memory, memory buffers, or digital indication(s)as used in each claims refers to the first or the second digital indication(s), first or second memory, or first or second memory buffers.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1, 19 - 23, 25 - 28, 30, 31, 33 - 36, 39 - 42, and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima, USPN 6,333,737 B1.

Claim 1

Nakajima teaches a method comprising providing a storage capacitor for each pixel. Nakajima, col. 1, lines 13 – 21; col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and figure 1. Nakajima teaches providing a memory 22 for each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a. Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claims 19, 26, 33, and 40

Nakajima teaches a pixel 2 for a liquid crystal display. Nakajima, figures 1 and 2; col. 2, lines 44 – 47; and col. 3, lines 11 – 17. Nakajima teaches providing a storage capacitor for each pixel. Nakajima, col. 1, lines 13 – 21; col. 2, line 67 – col. 3, line 5; col. 3, lines 22 – 25; and

figure 1. Nakajima teaches providing a first memory [memory 22] for each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1a.

Nakajima teaches providing a second memory [input circuit 38] separate from the first memory to store a second digital indication ["display data composed of digital signals input from the external"] of an updated voltage. The second digital indication is communicated [through the first data input line 32] from the second memory to the pixel cell. Nakajima, col. 5, lines 4 – 9.

Nakajima teaches a digital to analog conversion circuit 25 at each pixel. Nakajima, col. 3, lines 11 – 17; col. 6, lines 13 – 24; and figure 1. Nakajima does not specifically describe converting the digital indication into an analog voltage during a refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claims 20, 27, 34, 42

Nakajima teaches controlling the output from the second memory. Nakajima, col. 4, line 66 – col. 5, line 26.

Claims 21, 28,

Nakajima teaches that the first memory 22 is local to the pixel cell and the second memory [input circuit 38] is a global memory for multiple pixel cells. Cf. Nakajima, figures 1 and 2.

Claims 22, 30, 36, 44

Claim 22 is dependant on claim 19, wherein the memory comprises a static random access memory. Nakajima teaches that the memory may be a RAM. Nakajima, col. 3, lines 57 – 59.

Claim 23

Nakajima adds the step of reading the digital indication from the memory. Nakajima, col. 3, line 66 – col. 4, line 4; and col. 5, lines 51 – 52. Nakajima does not specifically describe the reading during the refresh operation, but it is inherent to the operation of such a circuit that the information would be changed during a refresh operation. See Nakajima, col. 1, lines 13 – 19.

Claim 25, 35, 41

It is inherent to the operation of Nakajima that the refresh operation occurs at a different rate than the frame update operation. Nakajima specifically teaches,

> Further, if each pixel is provided with the output means for outputting data for displaying pixels (display data) on the basis of the processed data in addition to the operating means, the operational processing can be immediately performed on the data input to a pixel from the external or adjacent pixels to display the pixel concerned.

Nakajima, col. 2, lines 14 – 20. See also: Nakajima, col. 5, lines 17 – 26; col. 5, line 42 – col. 6, line 3.

Claim 39

Nakajima teaches a circuit for updating the memory with another predetermined voltage. Nakajima, col. 3, lines 52 – 56; and col. 5, lines 42 – 50.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 24, 29, 32, 37, 38, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima in view of Kinoshita et al, USPN 5,771,031.

Claims 24, 32

Claims 24 and 32 each add the step of latching the digital indication from the memory during the refresh operation. As understood in the art, latching is holding data in a circuit until other circuits are ready to change the latch circuit.

Nakajima does not specifically teach the step of latching the information from the memory.

Kinoshita teaches the step of latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method and circuits as taught by Nakajima with the latching method and circuit taught by Kinoshita. Like Nakajima, Kinoshita teaches a drive method for individual pixels of a flat panel display. Kinoshita, col. 1, lines 5 –8; and col. 3, lines 60 –65. Both Nakajima and Kinoshita teach many of the same parts including storage capacitors, CS, memory, and digital to analog converters. See e.g. Kinoshita, figures 1, 3 & 4; col. 4, lines 33 –36; col. 5, lines 64 – 66; col. 7, lines 14 – 21; and col. 8, lines 11 – 14. Both teach the need to individually drive each pixel array. Kinoshita, col. 1, line 10 – col. 2, line 37; and col. 2, lines 6 – 9. Kinoshita invites such combination by teaching,

> In the trend of resent years, the number of pixels in each horizontal pixel array is increased to improve the resolution of the active matrix LCD, and the word length of each pixel data is also increased to improve the precision of the gray scale. In order to increase the number of pixels and the word length, it is

> necessary for the signal line driving circuit to process the pixel data at a higher speed. However, if the processing speed of the signal line driving circuit is improved to its limit, it is difficult to drive all the signal lines within one horizontal scanning period.

Kinoshita, col. 1, lines 28 – 37. Kinoshita adds as the object of invention,

> An object of the present invention is to provide a flat-panel display device and a method of driving the same, which can maintain the memory capacity required for block-driving of each horizontal pixel array to be small.

Kinoshita, col. 2, lines 6 – 9. Kinoshita further adds,

> According to the aforementioned flat-panel display device and its driving method, pixel data items sequentially supplied from outside are divided into pixel-data blocks each consisting of the same number of pixel data items, equivalent to the number of pixels forming one pixel block. M pixel-data blocks are sequentially written in M memory sections, and the M pixel-data blocks stored in the M memory sections are read in parallel while writing is performed. These M pixel-data blocks are supplied to corresponding ones of the data supply buses. Therefore, the total memory capacity of the memory sections is smaller than a memory capacity required for storing all items of pixel data for one horizontal pixel array. Further, the memory capacity of the memory section is not significantly depend on the number of pixel data items for one horizontal array and the word length of pixel data. This enables an increase in the number of pixel data items for one horizontal pixel array and an increase in the word length while maintaining the memory capacity of the memory section to be small. As a result of this, it is possible to prevent costs for manufacturing a flat-panel display device from being increased due to block driving of the horizontal pixel array.

Kinoshita, col. 2, line 63 – col. 3, line 17. Kinoshita teaches that the memory can be reduced with its latching circuit. Kinoshita, col. 9, lines 59 – 67; and col. 10, lines 60 – 67.

Claims 29, 43

Kinoshita teaches that the capacitors are associated with a row of pixels. Kinoshita, col. 4, lines 19 – 22, lines 35 – col. 36, and lines 62 - 65.

Claim 37

Nakajima teaches an operating unit 23a to communicate information from the memory to register circuit 24. Nakajima, col. 5, lines 51 – 66; and figure 1. Kinoshita teaches the step of

latching the information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

Claim 38

Kinoshita teaches latches to latch information from the memory while the data is updated. Kinoshita, col. 6, lines 39 – 42; col. 6, lines 63 – col. 7, line 6; col. 7, lines 14 – 21, lines 46 – 67; and col. 9, line 59 – col. 10, line 67.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akiyama et al., USPN 5,977,940, teaches a memory for each pixel of a liquid display device.

Okumura et al., USPN 5,945,972, teaches each of the pixels comprises memory elements.

Crossland et al., USPN 5,339,090, teaches a smart pixel.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600